WHAT IS CLAIMED IS:

1. A semiconductor device having an SOI structure formed by a semiconductor substrate <1>, an embedded insulating layer <2> and an SOI layer <3>, comprising:

a plurality of element forming regions provided in said SOI layer, each formed with a prescribed element;

an isolation film <31> provided in an upper layer part of said SOI layer for isolating said plurality of element forming regions from each other;

a first conductivity type semiconductor region <11, 12> provided under said isolation film as part of said SOI layer, said semiconductor region being formed in contact with at least one said element forming region having a first conductivity type among said plurality of element forming regions; and

a first conductivity type body region <10> provided in said SOI layer and capable of being externally fixed in electric potential, said body region being in contact with said semiconductor region, wherein

said semiconductor region at least partially has a first conductivity type impurity region not mixed with an impurity of a second conductivity type different from said first conductivity type but doped by only an impurity of said first conductivity type.

2. The semiconductor device according to claim 1, wherein

said first conductivity type impurity region is formed in a region <36> reaching said at least one element forming region from said body region.

3. The semiconductor device according to claim 1, wherein

said isolation film at least partially has a second conductivity type impurity-free region containing no impurity of said second conductivity type.

4. The semiconductor device according to claim 3, wherein

said second conductivity type impurity-free region is formed in a region reaching said at least one element forming region from said body region.

5. The semiconductor device according to claim 3, wherein

said second conductivity type impurity-free region includes a region having a larger thickness than the remaining region in said isolation film.

6. The semiconductor device according to claim 1, wherein

said prescribed element includes a transistor, and a gate electrode <9> of said transistor is formed to extend on said isolation film.

7. The semiconductor device according to claim 1, further comprising:

a dummy region <73, 74> formed in said SOI layer not to function as an element.

8. The semiconductor device according to claim 7, wherein

said dummy region includes a region where impurities of both of said first conductivity type and said second conductivity type are introduced.

9. The semiconductor device according to claim 7, wherein

said dummy region includes a first dummy region <72> where an impurity of

said first conductivity type is implanted and no impurity of said second conductivity type is implanted and a second dummy region <71> where an impurity of said second conductivity type is implanted and no impurity of said first conductivity type is implanted.

10. The semiconductor device according to claim 1, wherein

said isolation film includes an isolation film having a thickness of not more than 50 nm.

11. A semiconductor device having an SOI structure formed by a semiconductor substrate <1>, an embedded insulating layer <2> and an SOI layer <3>, comprising:

a plurality of element forming regions provided in said SOI layer, each formed with a prescribed element;

an isolation film <31> provided in an upper layer part of said SOI layer for isolating said plurality of element forming regions from each other;

a first conductivity type semiconductor region <11, 12> provided under said isolation film as part of said SOI layer, said semiconductor region being formed in contact with at least one said element forming region having a first conductivity type among said plurality of element forming regions; and

a first conductivity type body region <10> provided in said SOI layer and capable of being externally fixed in electric potential, said body region being formed in contact with said semiconductor region, wherein

said isolation film at least partially has a region having a larger thickness than the remaining region.

12. A method of manufacturing a semiconductor device comprising steps of:

(a) preparing an SOI substrate formed by a semiconductor substrate <1>, an embedded insulating layer <2> and an SOI layer <3>;

(b) selectively forming an isolation film <31> in an upper layer part of said SOI layer while forming a first conductivity type semiconductor region <11, 12> in a lower layer part of said isolation film so that said isolation film separates said SOI layer into a plurality of element forming regions and at least one said element forming region has a first conductivity type and is formed in contact with said semiconductor region among said plurality of element forming regions;

(c) selectively forming a second conductivity type active region <5, 6> on the surface of said at least one element forming region; and

(d) forming a first conductivity type body region <10> capable of being externally fixed in electric potential in said SOI layer to be in contact with said semiconductor region, wherein

said step (c) is carried out for forming said active region by setting a block region <41 to 45> including said body region and a partial region of said isolation film to a region inhibiting introduction of an impurity of said second conductivity type and introducing said impurity of said second conductivity type into said SOI layer.

13. The method of manufacturing a semiconductor device according to claim 12, wherein

said step (c) includes a step of introducing an impurity of said second conductivity type into said SOI layer through a mask of a first resist film <51, 52> formed on said block region.

14. The method of manufacturing a semiconductor device according to claim 13, wherein

said at least one element forming region includes a region for forming a transistor,

said method further comprising:

(e) a step executed in advance of said step (c) for forming a gate electrode <9> of said transistor on said at least one element forming region, said gate electrode being formed to extend on said isolation film,

said step (c) including a step of introducing an impurity of said second conductivity type into said SOI layer through masks of said first resist film and said gate electrode.

15. The method of manufacturing a semiconductor device according to claim 14, wherein

said first resist film and said gate electrode are continuously formed on a region reaching said at least one element forming region from said body region.

16. The method of manufacturing a semiconductor device according to claim 12, wherein

said at least one element forming region includes a region for forming a transistor,

said method further comprising:

(e) a step executed in advance of said step (c) for forming a gate electrode <9> of said transistor on said at least one element forming region, said gate electrode being

formed to extend on part of said isolation film,

said step (c) including a step of introducing an impurity of said second conductivity type into said SOI layer through masks of a first resist film formed on said body region and said gate electrode.

17. The method of manufacturing a semiconductor device according to claim 16, wherein

said gate electrode is formed on a region reaching said at least one element forming region from said body region.

18. The method of manufacturing a semiconductor device according to claim 12, wherein

said step (c) includes a step of introducing an impurity of said second conductivity type into said SOI layer through a mask of a first resist film <62> having a first opening on said active region, and

said step (d) includes a step of introducing an impurity of said first conductivity type into said SOI layer through a mask of a second resist film <61, 63> having a second opening on said body region.

19. The method of manufacturing a semiconductor device according to claim 18, wherein

said second opening includes an opening provided substantially only on said body region.

20. The method of manufacturing a semiconductor device according to claim

18, wherein

said second opening includes an opening provided on said body region and part of said isolation film.

21. The method of manufacturing a semiconductor device according to claim 20, wherein

said second opening includes an opening provided on a region reaching said at least one element forming region from said body region.

22. The method of manufacturing a semiconductor device according to claim 18, wherein

said first resist film further has a first dummy opening <71> on a region other than said body region, said semiconductor region and said at least one element forming region, and

said second resist film further has a second dummy opening <72> on a region other than said body region, said semiconductor region and said at least one element forming region.

23. The method of manufacturing a semiconductor device according to claim 22, wherein

said first and second dummy openings are formed on the same position in the same shape.

24. The method of manufacturing a semiconductor device according to claim 22, wherein

said first and second dummy openings are formed without overlapping with each other.